Continuous MOSFET performance increase with device scaling: The role of strain and channel material innovations

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A simple model that links MOSFET performance, in the form of intrinsic switch delay, to effective carrier velocity in the channel is developed and fitted to historical data. It is shown that nearly continuous carrier velocity increase, most recently via the introduction of process-induced strain, has been responsible for the device performance increase commensurately with dimensional scaling. The paper further examines channel material innovations that will be required in order to maintain continued commensurate scaling beyond what can be achieved with process-induced strain, and discusses some of the technological tradeoffs that will have to be faced for their introduction.

1. Introduction

Conventional MOSFETs have proven to be remarkably scalable to gate lengths of about 60 nm, which are compatible with the 130-nm high-performance CMOS technology node. Intrinsic device performance up to this node has increased by about 17% per year, following an inverse gate-length ($1/L_g$) dependence commensurate with channel length decrease. This performance increase has relied in part on the steady increase of channel carrier velocity due to gate-length scaling combined with innovations, such as super-steep retrograde channel doping, and highly doped halos around very highly doped source and drain junctions. However, the intrinsic carrier transport properties in the channel material have remained constant, i.e. those of the relaxed silicon lattice; from the 90-nm node onward, additional innovations have been introduced to increase channel carrier mobilities, and hence allow continuation of velocity increase, by the imposition of process-induced strain in the silicon channel of otherwise conventional MOSFETs. The introduction of strain into the Si channel at the 90-nm node (see for example [1]) has been critical to increasing carrier mobility and velocity in the channel and maintaining historical CMOS performance trends. In Section 2 of this paper, a model is developed that quantitatively illustrates the relationship among carrier velocity, MOSFET drain current, and switching time. Carrier velocity is extracted from published data, and its historical progression is plotted as a function of gate length. From the analysis, it is clear that additional improvements in channel velocity and therefore in mobility will be required in order for commensurate scaling (delay inversely proportional to gate length) to continue. Section 3 reviews the status of research efforts to improve electron and hole mobility using heterostructures of strained Si and strained SiGe, on both bulk and on-insulator substrates. Section 4 contains a discussion of some remaining challenges associated with these heterostructure MOSFETs, and the paper concludes in Section 5.

2. Impact of velocity on MOSFET switching time

The drain saturation current in a MOSFET normalized to the channel width, I_D/W, can be approximated as follows:

$$(I_D/W) = Q_s' v = C'_{oxinv}(V_G - V_t)v, \quad (1)$$

where Q_s' is the channel charge areal density at the virtual source, C'_{oxinv} is the gate-to-channel capacitance per unit area at inversion, and v is the effective carrier velocity at the virtual source, which is thus defined as the point in the channel at which the charge density is given by $C'_{oxinv}(V_G - V_t)$. V_G is the applied gate–source

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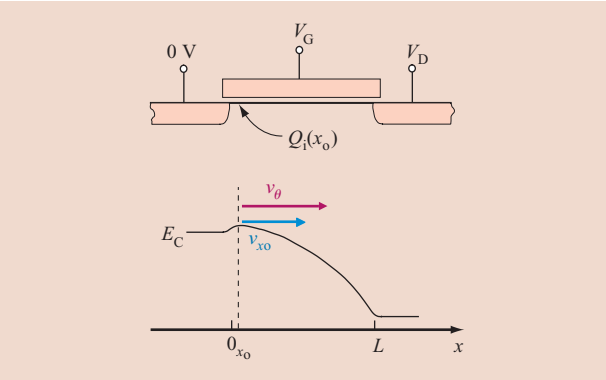

Figure 1

Illustration of the virtual source position x_o in the channel.

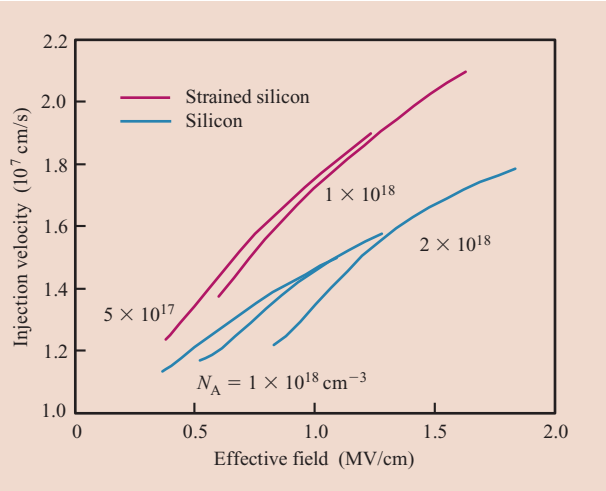

Figure 2

Calculated injection velocity v_θ vs. channel effective field for relaxed and ~1% biaxially strained bulk MOSFETs with different channel dopings. It was assumed that only the Δ_2 valleys are populated in simulating strained devices. The velocity would be even higher with uniaxial strain along the <110> direction because of the decrease in effective mass.

voltage, and V_t is the effective threshold voltage in saturation, i.e., obtained from linear extrapolation of the I_D–V_G curve to $I_D = 0$; V_t is given by

$$V_t = V_{t0} - \delta V_D , \tag{2}$$

where V_{t0} is the effective threshold voltage at drain-to-source voltage V_D, equal to zero, and δ is the drain-induced barrier-lowering (DIBL) coefficient. On the other hand, the intrinsic MOSFET switching delay, τ, is given by

$$\tau = \frac{\Delta Q_G}{I_{eff}} , \tag{3}$$

where ΔQ_G is the charge difference at the gate electrode between the two logic states, including both channel charge and intrinsic gate electrode fringing capacitance charge, and is given by

$$\Delta Q_G = C'_{oxinv} W (V_{dd} - V_t) + C^*_f V_{dd} , \tag{4}$$

and I_{eff} is the effective MOSFET switching current [2] given by

$$\begin{aligned} I_{eff} &= [I_D(V_G = V_{dd}/2, V_D = V_{dd}) \\ &\quad + I_D(V_G = V_{dd}, V_D = V_{dd}/2)]/2 \\ &= [Q'_s(V_G = V_{dd}/2, V_D = V_{dd}) \\ &\quad + Q_s(V_G = V_{dd}, V_D = V_{dd}/2)]v/2 \\ &= C'_{oxinv} W[(3 - \delta) V_{dd}/4 - V_t] . \end{aligned} \tag{5}$$

Using Equations (4) and (5) in (3) results in

$$\tau = \frac{V_{dd} - V_t + (C^*_f V_{dd}/C'_{oxinv} L_g)}{[(3 - \delta)/4] V_{dd} - V_t} \frac{L_g}{v} , \tag{6}$$

where V_{dd} is the supply voltage and C^*_f is the total effective gate fringing capacitance, including all internal and external fringing capacitances, with the Miller effect on the drain side taken into account. It is interesting to note that C^*_f is nearly independent of technology generation for properly scaled devices [3], with a value of about 0.5 fF/μm.

Because of the existence of finite resistance between the source contact (and the drain contact) and the channel, R_s, the actual carrier velocity at the virtual source, v_{xo}, can be approximated by

$$v_{xo} = \frac{v}{[1 - C'_{oxinv} R_s W (1 + 2\delta) v]} . \tag{7}$$

The virtual source point is located near the top of the potential barrier between source and channel, and v_{xo} is related to the so-called source injection velocity, v_θ, or ballistic-limit velocity, as discussed by Lundstrom [4]. **Figure 1** illustrates these concepts. Exact evaluation of v_{xo} has been described in [5]. The ballistic velocity v_θ for electrons vs. effective electric field in the channel is plotted in **Figure 2**, for both relaxed and strained Si using a self-consistent Schroedinger–Poisson solver, SCHRED [6]. For the strained Si it was assumed that only the Δ_2 valleys are populated, with no other changes relative to relaxed Si. The assumption that all electrons occupy the Δ_2 valleys corresponds roughly to an energy splitting between the Δ_2 and Δ_4 valleys greater than 140 meV, or a biaxial tensile strain level higher than approximately 1%.

While Equation (1) has been used primarily to model transistors in the ballistic limit, it actually fits state-of-the-

art transistor data over the period of the last two decades. Indeed, close examination of selected (bulk-Si) publications [7–15] allows v_{xo} for both electrons and holes to be tracked over the same period of time, for gate length L_g ranging from 480 nm to 35 nm. In those selected publications, C_{oxinv} is given or can be estimated accurately, δ can be extracted from the data, and R_s (or at least its upper bound) can be reasonably estimated from the output I–V characteristics near $V_D = 0$. In the data analyzed, values of the denominator in Equation (7) were typically higher than 0.80, indicating no more than ~20% correction to the raw extracted velocity, v. The values of v_{xo} extracted from the literature data are shown in **Figure 3**, as well as the required electron and hole velocities at $L_g = 10$ nm in order to continue the historical reduction of delay in direct proportion to L_g, as discussed below. As can be seen for both electrons and holes, the carrier velocity v_{xo} has been steadily increasing with decreasing L_g. For all gate lengths down to 60 nm, the channel is unstrained (100) silicon, and therefore the carrier mobility vs. effective field relationship has been essentially unchanged. The main reason for the general trend of velocity increase with scaling can be understood from the scattering theory [4] as being due to reduction of the characteristic length of the potential barrier near the source, as L_g is scaled, and therefore reduction of backscattering. This reduction in the characteristic length of backscattering has been the result of proper scaling of the electrostatic design of MOSFETs, and has been achieved via innovations in source/drain and channel doping engineering. The key point here is that v_{xo} should increase (provided v_{xo} is smaller than v_0) when there is a reduction in backscattering, either by reduction of the length over which backscattering can occur, which is the case here, or by reduction of the scattering rate. However, closer examination of the data shows that from $L_g \sim 130$ nm to 60 nm there has actually been a saturation of velocity increase that is most likely due to the increase of coulombic scattering near the source associated with increase in doping that counterbalances the decrease in the backscattering effective length.

Below 60 nm, the increase in velocity observed in Figure 3 is due to the introduction of well-known strain-induced mobility increases in the channel via innovative process steps [14, 15], which has brought about a decrease in the backscattering rate. With channel carrier mobility being a proxy for the inverse of the backscattering rate, it has been found experimentally via the application of strain that in short-channel devices there exists a ~0.5 ratio of proportionality between channel electron or hole velocity and mobility [1, 16]. An additional effect contributing to this proportionality ratio may also be the fact that the ballistic injection velocity increases because of the reduction in the carrier effective mass by applying

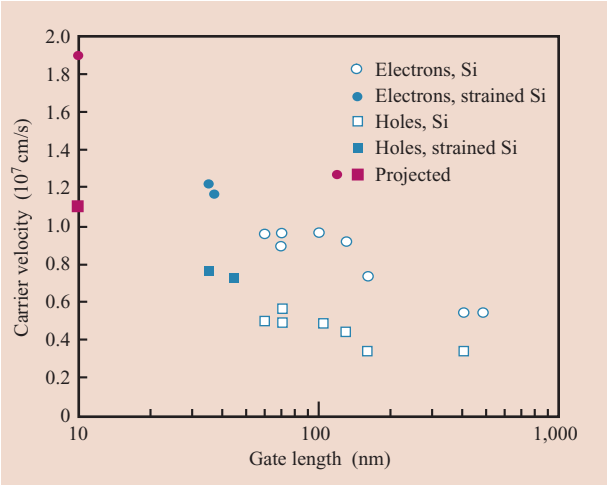

Figure 3

Calculated historical virtual source velocity v_{xo} of electrons and holes vs. gate length. Also shown are velocities at $L_g = 10$ nm that are required to continue the historical relation of intrinsic FET switching delay time to gate length. See text discussion and Figure 4.

strain. At first sight, it would appear that both n- and p-MOSFETs are approaching the ballistic limit after these innovations, but as Figure 2 shows (for electrons), this is not necessarily the case, because the injection velocity is also increasing. The electron injection velocity would be even higher with uniaxial strain along the <110> channel direction as a result of decreased effective mass [17].

MOSFET intrinsic delay calculated from extracted historical device data and Equation (5) is shown in **Figure 4** for n- and p-MOSFETs. Also shown are the projected intrinsic delays at $L_g = 10$ nm, using the corresponding extrapolated velocities of Figure 3 and making some more or less optimistically reasonable assumptions about device electrostatics (i.e., $\delta = 0.1$ V/V, subthreshold swing about 90 mV/decade resulting in $I_{off} \sim 300$ nA, at $V_{dd} = 0.8$ V. The last two values are from the 2004 International Technology Roadmap for Semiconductors (ITRS '04) [18] for $L_g = 10$-nm devices (22-nm high-performance node).

It is notable that historically the increase in velocity and therefore the steeper-than-L_g decrease of the L_g/v term has counterbalanced a parallel increase in the prefactor to that term in Equation (6), resulting in near-perfect proportionality between τ and L_g. Continuous improvement in intrinsic delay with scaling will require increasingly higher velocities, and at least for electrons in silicon, even with uniaxial strain, the velocity would have to approach the theoretical ballistic velocity as we approach 10-nm gate lengths. This would suggest that, at

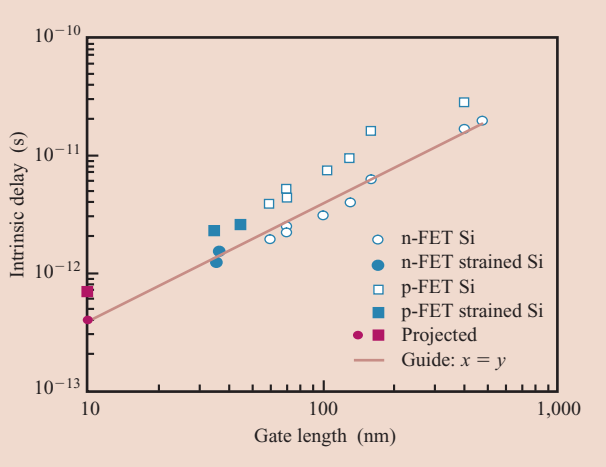

Figure 4

Calculated historical intrinsic FET switching delay time and gate length.

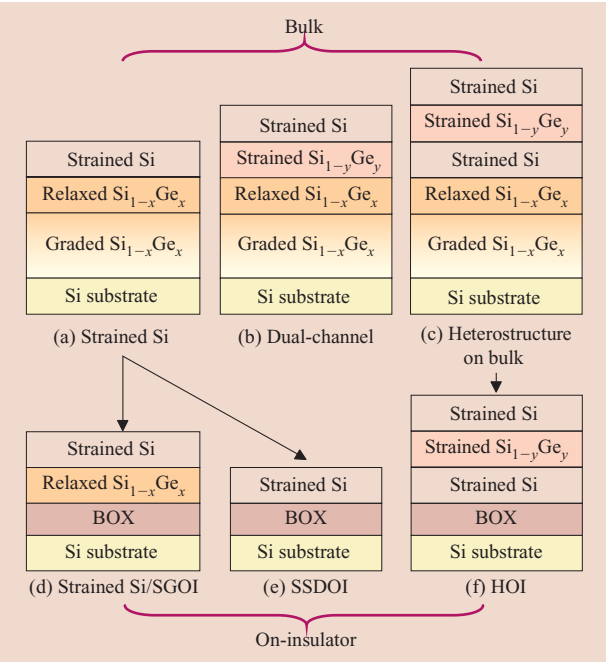

Figure 5

Schematic illustration of various heterostructure substrates used to investigate enhanced mobility, including bulk epitaxial technologies such as (a) biaxial strained Si on relaxed SiGe, (b) dual-channel structure ($y > x$), and (c) heterostructure on bulk; and on-insulator implementations on buried oxide (BOX) layers such as (d) strained Si/relaxed $Si_{1-x}Ge_x$ on insulator (SGOI), (e) strained Si directly on insulator (SSDOI), and (f) heterostructure on insulator (HOI). Arrows indicate the relationship between on-insulator substrates and their bulk counterparts.

least for n-FETs, this is not likely to happen in silicon channels.

It is clear from this discussion that the increase in channel carrier velocity results from backscattering reduction, and while some of it may result from further scaling of the characteristic length for backscattering, the channel mobility increase is, from this point in time onward, the main lever for continuing the historical decrease of transistor delay τ in proportion to L_g. Prospects for continued channel mobility increase are discussed in the following sections.

3. Strain and new channel materials

Although process-induced stress has been used to achieve significant mobility enhancements in short-channel devices (e.g., ~2x for holes in 65-nm technology [15]), the Si/SiGe materials system has the potential to achieve very large improvements in mobility (e.g., ~10x hole-mobility enhancements for strained Ge channels), as discussed below. The following two sections review the status of research on Si/SiGe heterostructure MOSFETs in bulk and on-insulator technologies.

Si/SiGe heterostructures on bulk

Figure 5 schematically illustrates various heterostructure substrates that have been used to investigate biaxial strain and high-mobility channel materials, including epitaxial structures on bulk substrates and on-insulator implementations. The on-insulator ("OI") substrates are generally derived from bulk structures by a combination of epitaxial growth, wafer bonding, and delamination or etch-back methods, which preserve the strain state of the layers. For example, strained silicon directly on insulator (SSDOI), illustrated in Figure 5(e), is derived from biaxial strained Si/relaxed $Si_{1-x}Ge_x$ by transfer of the epitaxial layers and removal of the relaxed $Si_{1-x}Ge_x$ virtual substrate, leaving a strained Si layer directly in contact with silicon dioxide [19–21]. The on-insulator technologies provide a pathway to implementing mobility enhancement in partially or fully depleted devices, in ultrathin-body MOSFETs, or nonplanar (e.g., double-gate) MOSFETs, and are discussed in the next subsection. This section focuses on the investigation of mobility in bulk MOSFETs.

Figure 6 compares effective mobility in bulk MOSFETs for (a) electrons in strained Si/relaxed SiGe and (b) holes in Si-channel and strained Si/$Si_{1-y}Ge_y$ dual-channel heterostructures. Dual-channel heterostructures [Figure 5(b)] use a combination of strained Si and strained $Si_{1-y}Ge_y$ to enable simultaneously high electron and hole mobilities [23–25]. In addition, because of the high Ge content and compressive strain, these structures offer significantly higher hole mobility than either biaxial-tensile strained Si [Figure 6(b), ○] or process-induced

strained Si [Figure 6(b), □]. As illustrated in Figure 6(b), the hole mobility increases with increasing Ge fraction in the strained $Si_{1-y}Ge_y$ channel. A hole-mobility enhancement factor of approximately 10x, relative to unstrained Si, is obtained for a p-MOSFET with a thin strained Si layer (~5 nm) on top of a strained Ge channel (~12 nm) on a relaxed $Si_{0.5}Ge_{0.5}$ virtual substrate [25]. The electron mobility in the strained Si channel is

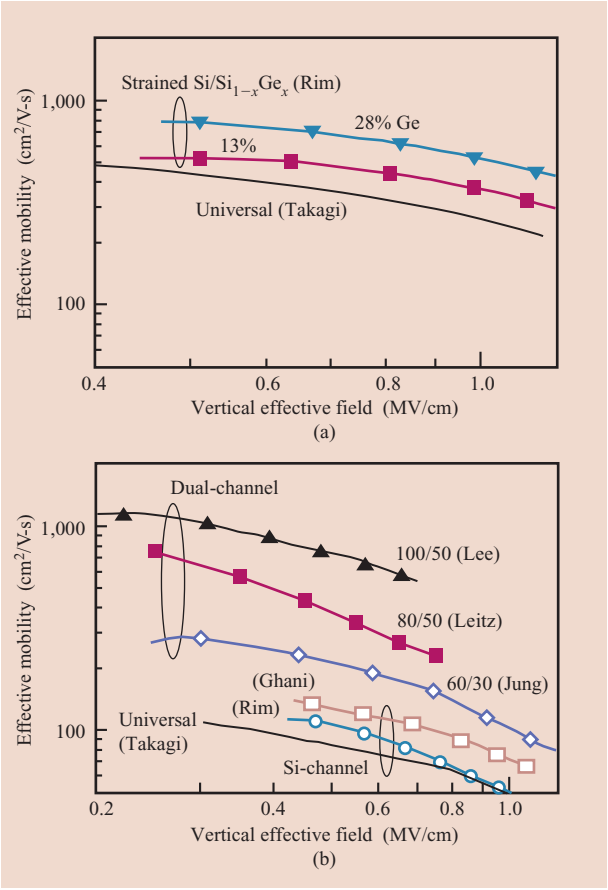

Figure 6

Comparison of MOSFET effective mobility in bulk technologies for (a) electrons in strained Si/relaxed $Si_{1-x}Ge_x$, and (b) holes in various Si-channel and strained Si/strained SiGe dual-channel implementations. For the strained Si channel p-MOSFETs, the data from Rim et al. is for biaxial strained Si/relaxed $Si_{1-x}Ge_x$ (28%) [22], and the data from Ghani et al. is for process-induced compressively strained Si implemented by the growth of SiGe in the source/drain regions [1]. For dual-channel structures, the notation y/x represents the Ge percentage in the strained $Si_{1-y}Ge_y$ layer and in the relaxed $Si_{1-x}Ge_x$ substrate, respectively. The highest hole mobility is obtained for a pure Ge channel strained in biaxial compression to a relaxed $Si_{0.5}Ge_{0.5}$ substrate [25]. Other dual-channel data is from Leitz et al. [23] and Jung et al. [24]. The curves marked "Universal" are for unstrained Si, from Takagi et al. [26].

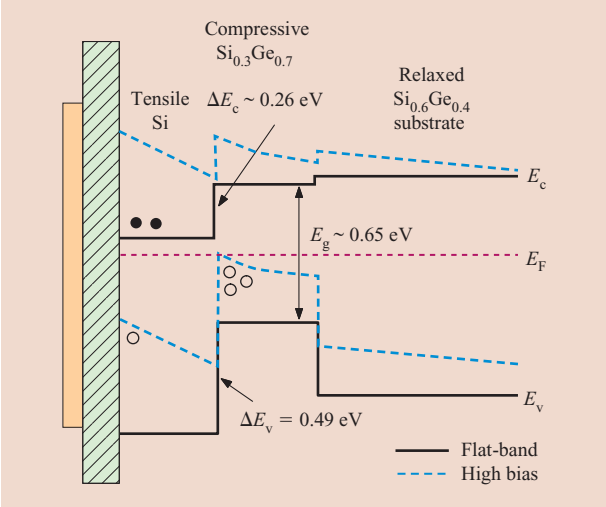

Figure 7

Energy band lineup for bulk p-MOSFETs fabricated in 70/40 dual-channel heterostructures, for bias conditions near flat-band (solid lines) and at high gate bias (dashed lines). Due to the band lineup, an electron inversion layer forms in the strained Si layer in the n-MOSFET, while hole inversion occurs first in the high-mobility strained SiGe layer, and at higher gate bias in the strained Si cap layer. Band offset values derived from Ni Chleirigh et al. [31].

enhanced by approximately a factor of 2 for the same structure. The high hole mobility results from a combination of the small Ge in-plane hole effective mass, the biaxial-compression-induced strain splitting of the valence bands, and the use of a thin Si cap layer, which enables a low interface state density to be obtained at the semiconductor/insulator interface. In Ge surface-channel MOSFETs, where the gate dielectric is formed directly on Ge without an intermediate Si layer, reported hole-mobility enhancements are in the range of 1.4 to 2x [27–29], and n-MOSFET performance is disappointing [30]. The use of Si-compatible gate insulator technology makes the strained Si/strained Ge dual-channel heterostructure very attractive.

Detailed understanding of dual-channel MOSFET operation requires information on the energy bands for the heterostructure. The energy band lineup for bulk 70/40 dual-channel p-MOSFETs is illustrated schematically in **Figure 7** (the notation y/x represents the Ge percentages in the strained $Si_{1-y}Ge_y$ layer and in the relaxed $Si_{1-x}Ge_x$ substrate, respectively). The large valence band offset (~0.5 eV) confines holes to the high-mobility strained $Si_{1-y}Ge_y$ channel. Due to the band lineup, an electron inversion layer forms in the strained Si layer in the n-MOSFET, while in the p-MOSFET, hole inversion occurs first in the high-mobility strained SiGe

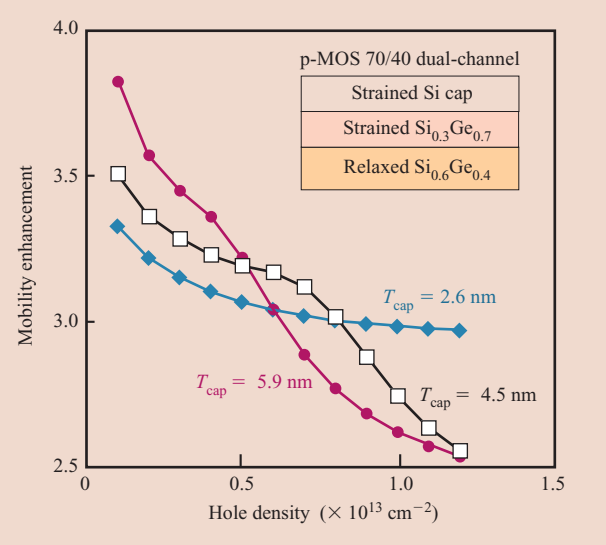

Figure 8

Measured effective hole-mobility enhancement factor relative to Si control devices for 70/40 dual-channel heterostructure p-MOSFETs with $Si_{0.3}Ge_{0.7}$ layer thickness ~ 10 nm. The mobility enhancement at high inversion charge densities is largest for thin strained Si cap layer thicknesses, T_{cap}, where the holes primarily populate the high-mobility strained $Si_{0.3}Ge_{0.7}$ layer. The Si cap thickness was extracted on each device by fitting measured C–V characteristics, as discussed in the text. The 3-nm-thick gate oxide was grown at 600°C, and the source/drain anneal was 800°C for 10 s. The data is for ring-structure MOSFETs with W = 1,000 μm and L = 50 μm.

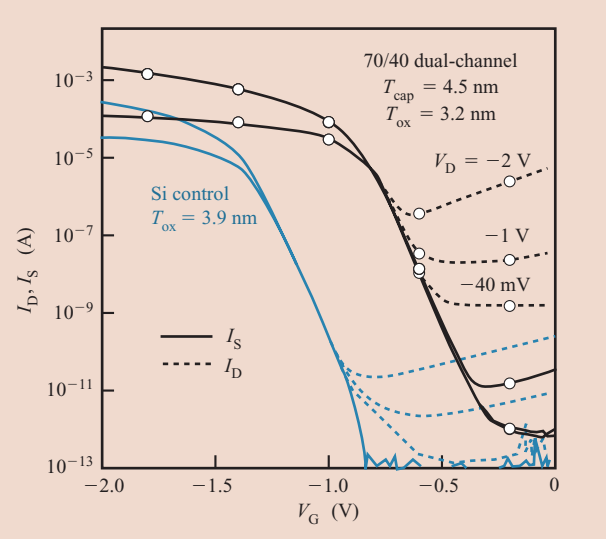

Figure 9

Comparison of measured subthreshold characteristics for 70/40 dual-channel and Si control p-MOSFETs (W = 1,000 μm, L = 50 μm, n^+ polysilicon gate). Subthreshold swing is 72 mV/decade for both devices. The threshold voltage is smaller for the dual-channel devices because of the narrower bandgap of the heterostructure. Off-state leakage is higher in dual-channel MOSFETs compared with control devices. From [32], reproduced with permission; ©2005 IEEE.

layer, and, at higher gate overdrive, in the strained Si cap layer, assuming a sufficiently thick Si cap layer. If the Si cap is thin (~2 nm), holes can be forced into the $Si_{1-y}Ge_y$, resulting in high mobility even at high inversion charge densities. The impact of the Si cap thickness on mobility is illustrated in **Figure 8**, which shows the measured hole-mobility enhancement factor, relative to Si control devices, for 70/40 dual-channel p-MOSFETs [32]. For the thinnest Si cap, mobility enhancements of 3x are obtained at all inversion charge densities measured (up to 1.3×10^{13} cm^{-2}). The Si cap thickness was extracted on each device by fitting simulations to measured capacitance voltage (C–V) characteristics, as discussed in the next subsection.

A challenge for these structures is illustrated in **Figure 9**. Measured off-state drain current is higher for dual-channel p-MOSFETs than for similarly processed Si control devices. The leakage occurs in the drain/gate overlap region, and the temperature dependence suggests a combination of band-to-band and trap-assisted tunneling [32]. The leakage increases with increasing Ge fraction, x in the substrate and y, in the $Si_{1-y}Ge_y$ channel, consistent with a reduction in the bandgaps of the strained Si and SiGe channel layers [32]. Drain leakage has also been observed in narrow-bandgap pseudomorphic Si/Ge/Si p-MOSFETs grown on unstrained Si [33]. These authors report reduced leakage for ultrathin Ge channels (~3 nm), though this also reduces the mobility enhancement. Detailed understanding requires further investigation, especially of the material quality in the ion-implanted gate/drain overlap region, which is subject to damage-enhanced interdiffusion of the Si and SiGe [34]. Optimization of the process should reduce trap densities in this region and the off-state leakage. Although the narrow bandgap of high-Ge-content SiGe may be associated with increased leakage, the reduction in the "effective bandgap" of the heterostructure (the energy difference between E_c in strained Si and E_v in strained SiGe, illustrated in Figure 7), relative to unstrained Si, has a positive implication: A single metal gate material, with a workfunction near the "mid-gap" of the heterostructure, may be utilized for both n- and p-MOSFETs, yielding appropriate threshold voltages [35, 36].

A remaining challenge of these structures is the fact that the p-MOSFET, even with a 1-nm-thick Si cap layer, is not strictly a surface-channel device, and thus the electrostatics are somewhat compromised. For heavily

doped substrates and thin gate oxides, this results in a larger subthreshold swing than observed for Si control devices [37]. The ideal subthreshold swing is recovered when the heterostructures are fabricated into fully depleted on-insulator MOSFETs, as discussed below. Simulations of the scalability of these structures are discussed in the following subsection.

Strained heterostructures on insulator

Strained Si/strained SiGe heterostructure on insulator (HOI) combines the transport benefits of the dual-channel structure with the electrostatics of fully depleted SOI (FD–SOI), and the potential to scale the body thickness into the ultrathin regime. To fabricate HOI, strained Si/strained SiGe/strained Si is grown on relaxed $Si_{1-x}Ge_x$, and the top three layers are transferred to the insulator, with the original strain state preserved in the transfer process, as illustrated in **Figure 10** [38]. A similar process may be used to fabricate strained Si directly on the insulator, with "x% SSDOI" referring to the Ge fraction of the relaxed $Si_{1-x}Ge_x$ in the donor substrate. In HOI, the strained Si on either side of the SiGe layer reduces the interface state density at the semiconductor/dielectric interface, compared with devices in which the SiGe is in direct contact with the oxide (see for example [39] for a discussion of SiGe/oxide interface quality). In HOI, the lower strained Si layer also has the potential to serve as a second (bottom) channel for electrons, in double-gate structures. The top strained Si layer serves as the electron channel in the n-MOSFET, and it can be selectively thinned to a thickness of 1 to 2 nm on the p-MOSFET to enable near-surface-channel operation with Si-compatible gate dielectric technology.

HOI has been fabricated with up to 55% Ge in the $Si_{1-y}Ge_y$ channel, and donor-wafer relaxed SiGe layers with Ge content of 25% ("55/25 HOI") [40]. A reduced thermal budget process is used for both substrate fabrication (maximum bond anneal 600°C, 2.5 hr) and MOSFET processing (600°C, 5-hr gate oxidation, and 800°C 10-s source/drain activation) [40]. As in dual-channel MOSFETs, control of the strained Si cap thickness is critical to the operation of HOI MOSFETs. The Si cap thickness on the p-MOSFET can be extracted from a combination of *C–V* measurements and simulations, as illustrated in **Figure 11**. Calculations using the Dessis simulator [42] are employed, and quantum effects are taken into account using the density gradient correction model, with density of state values modified for strained Si and models verified on bulk dual-channel devices [31]. **Figure 12(a)** shows simulated hole-density distributions as a function of distance from the strained Si/SiGe interface, in 46/25 HOI. As illustrated in the figure, thin Si cap layers (~2 nm) result in a hole

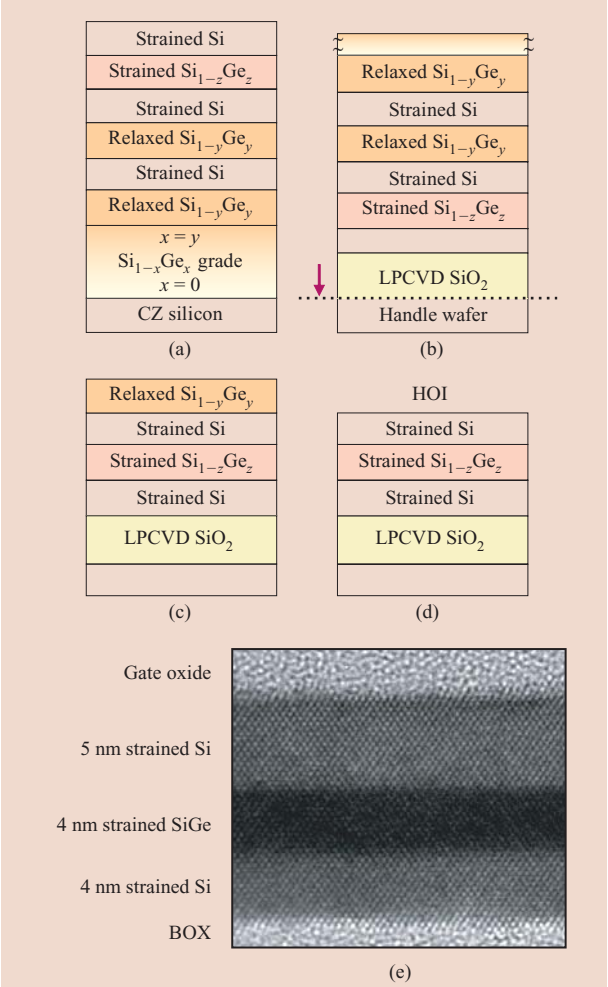

Figure 10

Fabrication process for HOI, illustrating the layer structure (a) as grown; (b) after deposition of low-temperature oxide, planarization, bonding, grind-back and TMAH etch (the arrow marks the location of the bond interface); (c) after selective etch, stopping on the Si layer, and removal of the Si etch stop; (d) after SC-1 removal of the $Si_{1-y}Ge_y$ etch-stop layer, resulting in the HOI structure (from [38], reproduced with permission; ©2004 IEEE); SSDOI is fabricated by a similar process, without growth of the strained $Si_{1-z}Ge_z$ layer. (e) Cross-section transmission electron micrograph (XTEM) of a 55/25 HOI structure after MOSFET fabrication.

distribution that is primarily in the high-mobility, compressively strained SiGe, even at high inversion charge densities of 10^{13} cm^{-2}. Such thin-cap HOI devices enable constant hole-mobility enhancement as a function of inversion charge density, illustrated in **Figure 12(b)**.

Figure 13 compares electron and hole mobilities in SSDOI and HOI [40]. Mobility in co-fabricated SOI control devices is close to the published universal mobility curves (dashed lines) [26]. For electrons [Figure 13(a)],

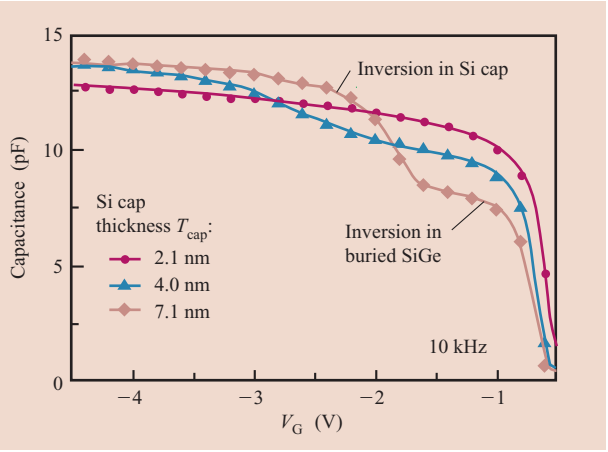

Figure 11

Measured (symbols) and simulated (curves) gate-to-channel inversion capacitance for 46/25 HOI p-MOSFETs (T_{ox} = 3.5 nm, n^+ polysilicon gates). Simulations are from [42] using the density gradient quantum correction model with default parameters. As is consistent with the band lineups illustrated in Figure 7, for the thicker-cap devices, the inversion layer forms in the buried SiGe at low gate overdrives and in the strained Si cap layer at higher overdrives. For the 2.1-nm-thick cap device, the Si cap is too thin to accommodate the holes, and inversion occurs primarily in the SiGe layer, resulting in a slight decrease in the maximum capacitance or an increase in the effective insulator thickness. From [41], reproduced with permission; ©2004 IEEE.

mobilities in HOI and in corresponding SSDOI are similar, though slightly degraded in HOI, perhaps associated with the finite Si cap thickness (5 nm) and the impact of Ge from the underlying SiGe layer, which is absent in SSDOI. For holes [Figure 13(b)], very high strain levels (e.g., 40% SSDOI) are required to achieve hole-mobility enhancement in tensile-strained Si at high inversion charge densities, N_{inv}. This can be explained by quantization effects that reduce the strain-induced splitting of the valence bands in strong inversion, for the case of biaxial tensile strain in Si [44, 45]. In compressively strained Si (biaxial or uniaxial), quantization effects are not expected to counteract the strain-induced valence band splitting; thus, hole-mobility enhancement should be relatively constant with increasing inversion charge density (as observed in p-MOSFETs with Si channels under compressive stress [46]). When compressive stress is applied to SiGe, constant hole-mobility enhancement may also be expected with inversion charge density, because of the similarity of the Si and SiGe valence band structure. Indeed, as illustrated in Figure 13(b), the hole-mobility enhancement in compressively strained 46/25 HOI is maintained at large inversion charge density, and is significantly larger than that observed in 40% SSDOI.

Figure 14 compares long-channel subthreshold characteristics for 25% SSDOI and 55/25 HOI n- and p-MOSFETs. Low subthreshold swing is achieved in fully depleted HOI MOSFETs in spite of the buried SiGe channel, an advantage compared with bulk dual-channel heterostructure devices [37]. The issue of elevated off-state leakage relative to SSDOI or SOI control devices, discussed above for bulk heterostructures, remains in

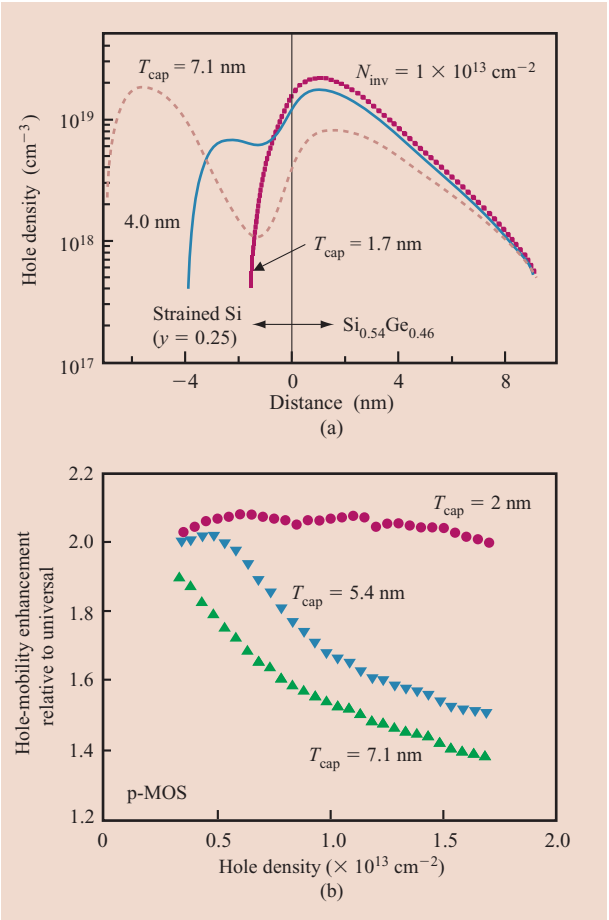

Figure 12

In 46/25 HOI, (a) simulated hole density as a function of distance from the strained Si/SiGe interface, for three Si cap-layer thicknesses; (b) measured hole-mobility enhancement factors. In (a) the total integrated inversion charge density, N_{inv}, is fixed at 10^{13} cm^{-2}. The thicker cap devices show separate inversion-layer formation in the SiGe and Si layers. For the 1.7-nm-thick cap device, hole inversion occurs primarily in the SiGe even at high inversion charge density. This is evident in the higher mobility at high inversion charge densities for the devices with thin strained Si caps shown in (b), where enhancement factors are taken relative to the universal curve derived from Takagi [26]. From [41], reproduced with permission; ©2004 IEEE.

HOI. Thinning the SiGe layer from 10 nm to 4 nm reduces the off-state leakage by roughly a factor of 3, but the mobility is also reduced, as illustrated in **Figure 15** [40]. Further study of the leakage mechanisms is required in order to understand the tradeoffs between enhanced mobility and drain leakage.

The behavior of these new heterostructure materials in short-channel devices requires investigation. The electrostatics for the p-MOSFET have been simulated to evaluate the impact of the heterostructure on scalability.

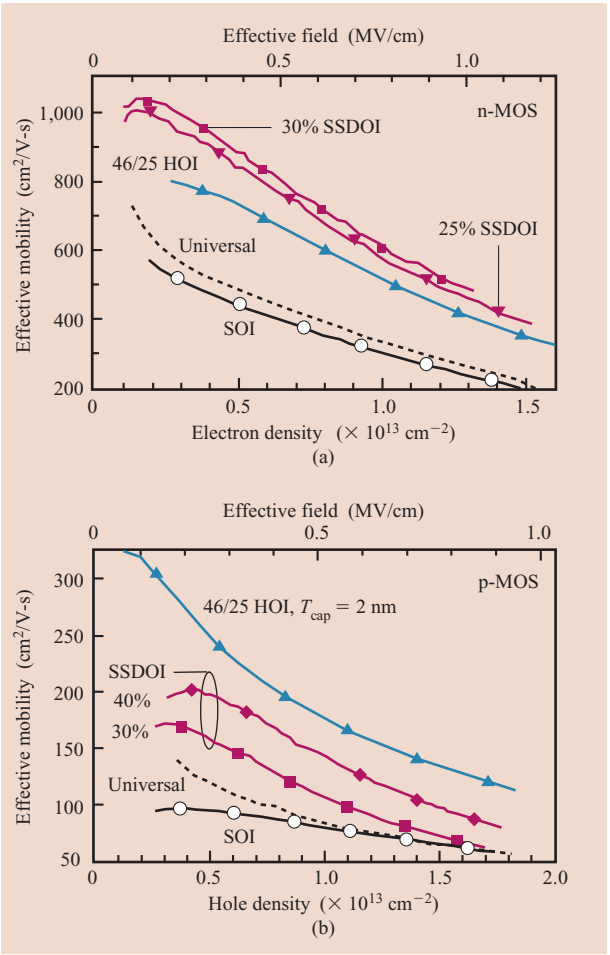

Figure 13

Comparison of measured effective mobility in SSDOI (10- to 20-nm body thickness), SOI, and HOI for (a) electrons, (b) holes. Mobility in lightly doped SOI control devices is close to the published universal mobility from [26]. Due to the simplicity of the contact and source/drain processes, a Kelvin mobility-extraction MOSFET [43] with $L = 100\ \mu$m was used to enable accurate mobility extraction even with the high parasitic resistance of thin-body devices. From [40], reproduced with permission; ©2006 IEEE.

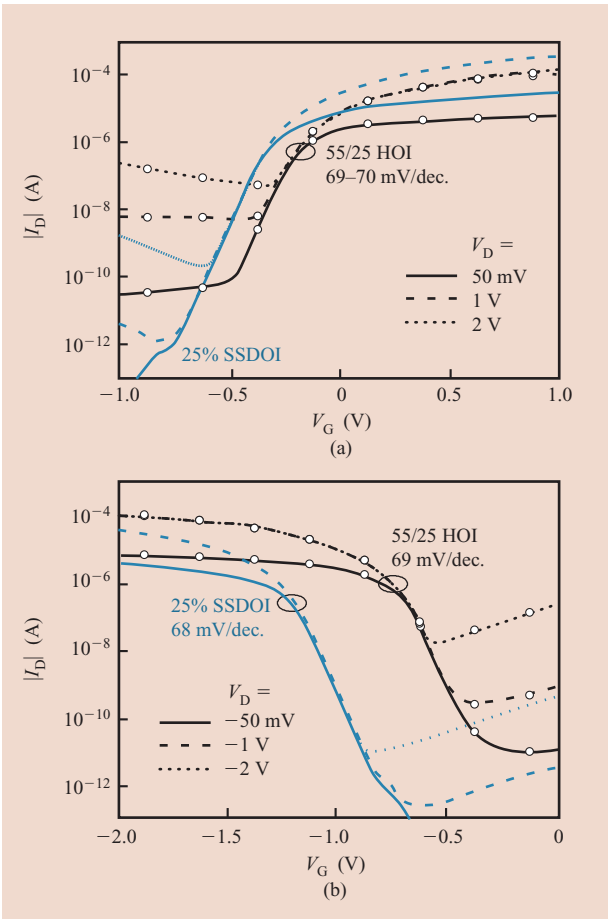

Figure 14

Measured subthreshold characteristics for (a) n-MOSFETs and (b) p-MOSFETs ($W = 50\ \mu$m, $L = 50\ \mu$m, $T_{ox} = 4$ nm, n^+ polysilicon gates) fabricated in SSDOI and 55/25 HOI. The body thickness for both the SSDOI and HOI MOSFETs is ~20 nm. For HOI, the body thickness includes the 10-nm-thick SiGe layer and the surrounding strained Si layers. The strained Si cap thickness (3–5 nm) and band structure differences between strained Si and SiGe result in threshold voltage shifts between the SSDOI and HOI MOSFETs. Differences in parasitic resistance make direct comparison of the on-state currents difficult. As for bulk heterostructures, off-state leakage is higher in HOI than in SSDOI or SOI control devices (not shown). From [40], reproduced with permission; ©2006 IEEE.

Figure 16 compares simulated subthreshold swing (SS) for 46/25 HOI and SOI p-MOSFETs of equal body thickness, assuming 1-nm-thick Si cladding layers on either side of the SiGe layer (i.e., $T_{body} = 1$ nm Si + T_{SiGe} + 1 nm Si). The physical device parameters were taken from the International Roadmap for Semiconductors (ITRS) [18], assuming a fixed equivalent oxide thickness of 1 nm. For gate lengths down to 20 nm, subthreshold swing in

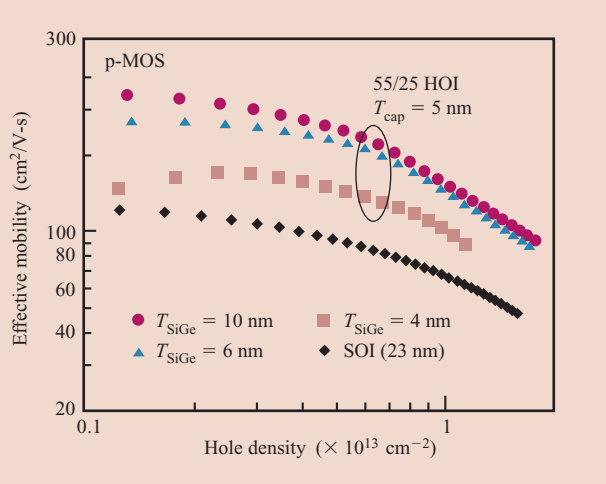

Figure 15

Measured hole mobility in 55/25 HOI with ultrathin strained SiGe channels, compared with SOI control devices. In the HOI, the top and bottom strained Si layers are 4 to 5 nm thick, as illustrated by the XTEM in Figure 10. When the thickness of the buried SiGe layer is reduced, the hole mobility decreases, particularly for the devices with a 4-nm-thick SiGe layer. From [40], reproduced with permission; ©2006 IEEE.

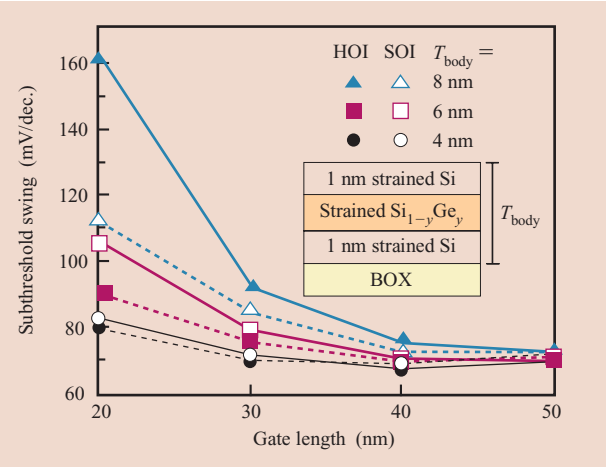

Figure 16

Simulated subthreshold swing (SS) for 46/25 HOI and SOI p-MOSFETs for body thicknesses T_{body} of 8, 6, and 4 nm, assuming 1-nm-thick Si cladding layers on either side of the SiGe layer (i.e., T_{body} = 1 nm Si + T_{SiGe} + 1 nm Si). The doping in the semiconductor was fixed at 10^{17} cm^{-3} and the device physical parameters were taken from the ITRS [18], assuming an equivalent oxide thickness of 1 nm. The source/drain doping profile gradient was taken to be 2 nm/dec., and the gate length L_{eff} is defined by the points where the source/drain doping reaches 2 × 10^{19} cm^{-3}. The density gradient model was used in [42], with parameters calibrated from Schrödinger solutions.

HOI is only slightly increased (~15%), compared with that for SOI, for total film thicknesses T_{body} less than or equal to 6 nm. This SS increase originates from the decreased semiconductor capacitance associated with the displacement of the hole charge centroid from the oxide/semiconductor interface. When the body thickness is comparable to the inversion layer thickness (e.g., 4 nm), the subthreshold swing of the HOI device approaches that of the SOI device. At this thickness, however, the hole-mobility enhancement is expected to decrease as the SiGe channel layer is thinned. Investigation of transport in short-channel devices incorporating these new materials is a topic for future research.

4. Discussion and future opportunities

Although the mobilities achieved in long-channel strained Si/strained SiGe heterostructures on bulk and insulator are promising, there are significant practical challenges associated with implementing these materials in a manufacturable CMOS technology, including material quality of the as-grown epitaxial layers, process integration issues such as interdiffusion between thin Si and SiGe layers, and the potential for formation of defects in strained layers during processing. Progress in these challenging areas has been achieved. Significant improvements have been demonstrated in reducing the defect densities in relaxed SiGe layers on Si substrates [47]. Interdiffusion at Si/SiGe interfaces is being studied and limits the thermal budget as the Ge content is increased because of the strong dependence of the interdiffusivity on Ge fraction and strain [48]. Laser annealing may be a solution to this issue. Enhanced diffusion of dopants along misfit dislocations at the strained Si/SiGe interface has been associated with increased off-state leakage in short-channel MOSFETs, and the strained Si thickness and Ge fraction in the SiGe layer must be limited, for a given thermal budget, to prevent this phenomenon [49, 50]. It should be noted that many of these challenges are associated with the presence of SiGe during CMOS processing, and that SSDOI thus has the potential for simpler process integration than HOI structures (but with less mobility leverage for p-MOSFETs).

Additional research on gate dielectric materials to be used with these structures is required. High-k dielectrics have been employed on strained Si surface-channel n-MOSFETs, and can be used to recover the mobility loss associated with high-k insulators such as HfO_2 on Si [22, 51]. A potential benefit of devices incorporating strained Si on SiGe is the possibility of reduced gate leakage currents, associated with the increased barrier height at the semiconductor/gate dielectric interface due to the strain-induced lowering of the conduction-band

energy [52]. An additional challenge for Ge-containing devices is the need for a high-quality high-k gate dielectric that can be formed *directly on* SiGe or Ge. High-k gate dielectrics (e.g., TiN gate electrode with HfO_2 dielectric) have been demonstrated directly on $Si_{0.7}Ge_{0.3}$, with 1.5x hole-mobility enhancement, but gate leakage currents were larger than for Si control devices [53]. Until a high-quality gate insulator for SiGe or Ge is developed, a thin (~1-nm) Si cap layer, which enables the use of Si-compatible gate technology, is a reasonable compromise for the p-MOSFET. High-k gate stacks with metal gate electrodes (TiN/HFO_2) have been demonstrated on strained SiGe channels, with thin sacrificial Si layers (~1 nm) used to improve the interface quality [36], and on MOSFETs incorporating strained Si (2.5 nm thick)/strained Ge (7 nm thick) on relaxed SiGe (50% Ge) with 9x hole-mobility improvement over Si control devices [54]. Thus, the use of high-k gate stacks with strained Si/strained Ge is expected to enjoy the same large mobility enhancements demonstrated in earlier work using SiO_2 gate dielectrics [25].

An area of interest for future work is the combined use of global and local stress techniques, for example by the application of process-induced stress (Si_3N_4 etch-stop liners over the gate) to devices containing initially biaxially strained Si or Ge channels. Such methods may offer larger enhancements than can be obtained from either process-induced or global stress techniques alone. This concept is illustrated in [55], where the impact of mechanical stress on SOI and SSDOI devices is studied. In that work, biaxial tensile strain in the Si is used to split the conduction-band degeneracy and repopulate all electrons into the Δ_2 conduction band. Superimposed on this stress is a uniaxial component along the [110] direction, induced by mechanical bending, which deforms the Δ_2 band, i.e., induces a change in the effective mass. Such effective mass changes are important in short-channel devices because of the impact of effective mass on the Coulomb-scattering-limited channel mobility.

The application of these enhanced-mobility materials to nonplanar devices, such as FinFETs or tri-gate structures, requires investigation. Patterning-induced changes in strain and mobility also require study. Patterning of initially biaxially strained SiGe films on insulator has been used to produce uniaxially strained SiGe p-MOSFETs with improved short-channel mobilities [56]. The passivation of SiGe heterostructures will remain an issue, since nonplanar devices inherently have a large surface-to-volume ratio. Finally, since InGaAs and related compounds have very high electron mobilities (of the order of 10,000 cm^2/V-s), these materials are attractive for investigation as high-performance n-FETs on Si substrates. When coupled with the high hole mobility in strained Ge, a III–V/Ge channel pair may be of interest for future n- and p-FET logic devices.

5. Summary and conclusions

A simple model that links MOSFET performance to effective carrier velocity in the channel has been developed and used to extract electron and hole velocities in Si MOSFETs from published electrical data. The impact of improved mobility associated with process-induced strain is evident from the extracted carrier velocities. From the analysis of carrier velocity and its effect on intrinsic device switching delay, it is clear that additional improvements in velocity (and hence channel mobility) beyond those that have been achieved with process-induced stress will be required in order for commensurate scaling (delay inversely proportional to channel length) to continue. Research on long-channel MOSFETs has demonstrated that significant mobility enhancements (e.g., 2x for electrons and 10x for holes) relative to Si MOSFETs can be achieved in the strained Si/strained SiGe materials system. On-insulator analogs of these bulk heterostructure devices (e.g., SSDOI and HOI) have been demonstrated, with encouraging mobility and subthreshold characteristics. Associated with these heterostructures are several fundamental tradeoffs, such as the mobility enhancement and the leakage current, both of which increase with Ge content. The heterostructure must be optimized with such tradeoffs in mind. There are also enormous practical challenges in implementing these heterostructures in a manufacturing technology. The higher mobility offered by SiGe, Ge, and III–V semiconductors on silicon, and the improvements in lattice-mismatched epitaxial growth, continue to make these heterostructures a promising and active area of device research.

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