LETTERS

'Memristive' switches enable 'stateful' logic operations via material implication

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The authors of the International Technology Roadmap for Semiconductors[1]—the industry consensus set of goals established for advancing silicon integrated circuit technology—have challenged the computing research community to find new physical state variables (other than charge or voltage), new devices, and new architectures that offer memory and logic functions[1–6] beyond those available with standard transistors. Recently, ultra-dense resistive memory arrays built from various two-terminal semiconductor or insulator thin film devices have been demonstrated[7–12]. Among these, bipolar voltage-actuated switches have been identified as physical realizations of 'memristors' or memristive devices, combining the electrical properties of a memory element and a resistor[13,14]. Such devices were first hypothesized by Chua in 1971 (ref. 15), and are characterized by one or more state variables[16] that define the resistance of the switch depending upon its voltage history. Here we show that this family of nonlinear dynamical memory devices can also be used for logic operations: we demonstrate that they can execute material implication (IMP), which is a fundamental Boolean logic operation on two variables *p* and *q* such that *p*IMP*q* is equivalent to (NOT*p*)OR*q*. Incorporated within an appropriate circuit[17,18], memristive switches can thus perform 'stateful' logic operations for which the same devices serve simultaneously as gates (logic) and latches[19] (memory) that use resistance instead of voltage or charge as the physical state variable.

In 1936, more than ten years before the discovery of the transistor, Claude Shannon invented digital electronics during his Master's thesis[20] research. He showed that the basic Boolean logic operations *p* OR *q* and *p* AND *q* could be implemented with simple electronic circuits that contained two switches in series (OR) and parallel (AND). By including the NOT operation, which could be implemented with a relay, Shannon proved that a small set of electrical components could be assembled to compute the result of any compound Boolean logic operation, that is, his choice of operations was computationally complete. This selection of logic operations has had a tremendous influence on the subsequent development of digital logic, but it was not unique. In their 1910 masterpiece *Principia Mathematica*, Whitehead and Russell[21] described four fundamental logic operations, the three later chosen by Shannon and one other that Russell regarded as particularly powerful and named 'material implication', *p*IMP*q* (that is, '*p* implies *q*' or 'if *p*, then *q*'). (Although material implication is seldom discussed within the electrical engineering and computing communities, it is in common use among logicians.) In fact, the IMP and FALSE operations (where the FALSE operation always yields the logic value 0) form a computationally complete logic basis (see truth table 1 in the Supplementary Information). We show here that material implication is naturally realized in a simple circuit combining a conventional resistor with two electrically connected memristors or memristive devices used as digital switches. Three memristors are sufficient to execute a NAND operation. As with Shannon's original formulation of digital logic, the physical representation or state for the logic value of a memristive IMP operation is the resistance of a switch. That makes IMP logic 'stateful': the memristive switches both store logic values and perform logic operations. The same nanoscale switches can be dynamically defined to be either logic gates or memory latches[19], so memristive IMP can be embedded within a nanoscale crossbar array to perform logic using the memory cells themselves.

Memristors[15] (a contraction of 'memory-resistor') and memristive devices[16] were predicted to exist by Chua in the early 1970s, but were not intentionally reduced to practice until 2008[13,14], when the link was made to voltage-polarity-dependent or bipolar-resistive switching phenomena, which have been observed for decades. These are dynamical devices with resistances that change over time as a function of their existing state and the voltages applied across them and/or currents driven through them. When operated with low voltages over short time intervals, they are analogue devices that display a controllable hysteresis in their current–voltage characteristic[13,22]. However, when overdriven by large voltages, they are essentially two-state digital switches or latches that can be opened (high resistance state) or closed (low resistance state) by the application of opposite polarity voltages.

Figure 1a shows a 1×17 crosspoint array of memristive switches formed in the junctions between one 50-nm-wide common bottom wire and seventeen top 50-nm wires. The idealized electrical switching characteristic for a single memristive device is illustrated in Fig. 1b: a positive voltage greater than an effective threshold V_{OPEN} applied for 2 μs toggles the junction from the low-resistance state (which we define as logical 1, opposite to the convention of Shannon) to the high-resistance state (0), while a negative voltage with magnitude larger than V_{CLOSE} performs the opposite operation. The experimentally measured switching properties of a single 50 nm × 50 nm device are shown in Fig. 1c and d. The junction is essentially non-volatile: there is negligible change of resistive state if the magnitude of the applied voltage remains small, but it undergoes a rapid and large resistance change if the voltage significantly exceeds either the V_{OPEN} or V_{CLOSE} effective thresholds for an interval longer than the corresponding switching time of the device. For the measurements reported in Fig. 1c and d, the series resistance of the millimetre-long but 50-nm-wide address wires drops a significant fraction of the externally applied voltage; this voltage drop increases the external voltage required for switching, reduces the switching ratio as seen from the drive electronics, and creates a large resistance–capacitance time constant that limits the speed of the measurements. Such a series resistance and parasitic capacitance would be dramatically reduced in a hybrid integrated circuit containing memristive switches and transistors in close proximity. Figure 1d shows the nano-device current versus the internal

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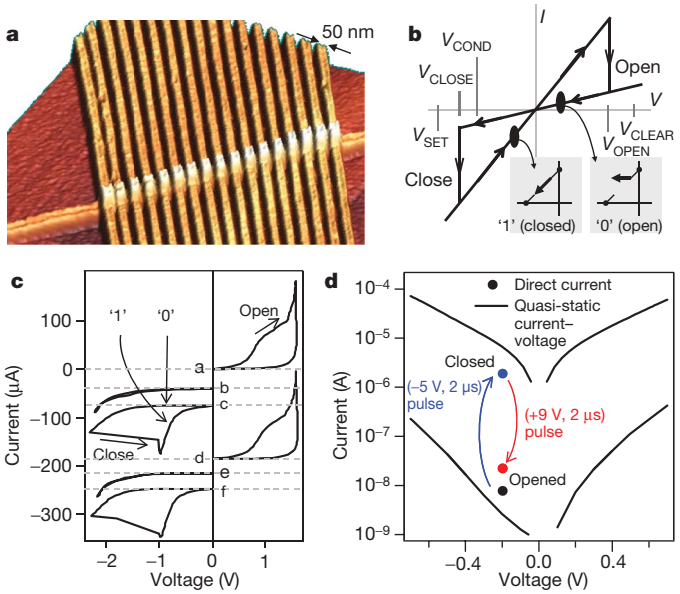

Figure 1 | Characterization of memristive switches. **a**, Atomic force microscope micrograph of a nanocircuit. **b**, Idealized memristive electrical characteristics, with abrupt voltage thresholds for opening and closing the switch between the low-resistance switch-closed state (logical value '1') and the high-resistance switch-open state (logical value '0'). **c**, Experimental direct-current current–voltage switching characteristics (four-probe method). Traces b–f are offset. Trace a shows a closed-to-open transition, trace b shows stability and trace c shows an open-to-closed transition. Traces d–f repeat this cycle. **d**, Switch toggling by pulsed voltages (2 μs long; $V_{SET} = -5$ V and $V_{CLEAR} = +9$ V). Non-destructive reads at −0.2 V test the switch state.

voltage across the junction (a four-wire measurement). In this system, 2-μs external voltage pulses of −5 V to close and +9 V to open yielded a switching resistance ratio >100 as measured at −0.2 V (Fig. 1d); this ratio was large enough to demonstrate the IMP operation within the nanoscale array.

The basic implication gate/latch circuit is shown in Fig. 2a. Two memristive devices, P and Q, are connected by a common horizontal nanowire to a load resistor, R_G, which is connected to the ground. We represent the states of P and Q by the logic variables p and q, respectively. The vertical nanowires (which form P and Q by crossing over the horizontal nanowire and a layer of memristive switching material) are controlled by tri-state voltage drivers that have a high-impedance output state when undriven. A given device may be 'set' (assigned a logic value of 1) by applying a negative voltage, V_{SET}, to its corresponding tri-state driver (this is the operation TRUE). To compensate for the voltage drop across the load resistor, R_G, the magnitude of V_{SET} is necessarily larger than V_{CLOSE}. Similarly, the device may be 'cleared' (assigned a logic value of 0; the operation FALSE) by applying a positive voltage, V_{CLEAR}. In other words, setting a memristive switch places it in a low-resistance state (logic 1), and clearing it places it in a high-resistance state (logic 0). We also define a negative voltage, V_{COND}, with a magnitude smaller than V_{SET}, which does not change the state of its driven device; its use will be shown shortly. We use the standard engineering notation '←' to represent synchronous state changes, so that $p \leftarrow x$ is read as 'the state of switch P (the logic value p) is changed to x the next time P is pulsed (by V_{SET}, V_{CLEAR} or V_{COND})'.

The key to performing an IMP operation with memristive switches is to understand the conditional toggling property that was first demonstrated for the crossbar latch[19]. The memristive IMP operation, $q \leftarrow p\mathrm{IMP}q$ (with p left unchanged), is implemented by simultaneously applying a V_{SET} pulse to Q and a V_{COND} pulse to P to execute a conditional switching condition. If V_{SET} is applied to Q alone, it executes the unconditional operation $q \leftarrow 1$, while the

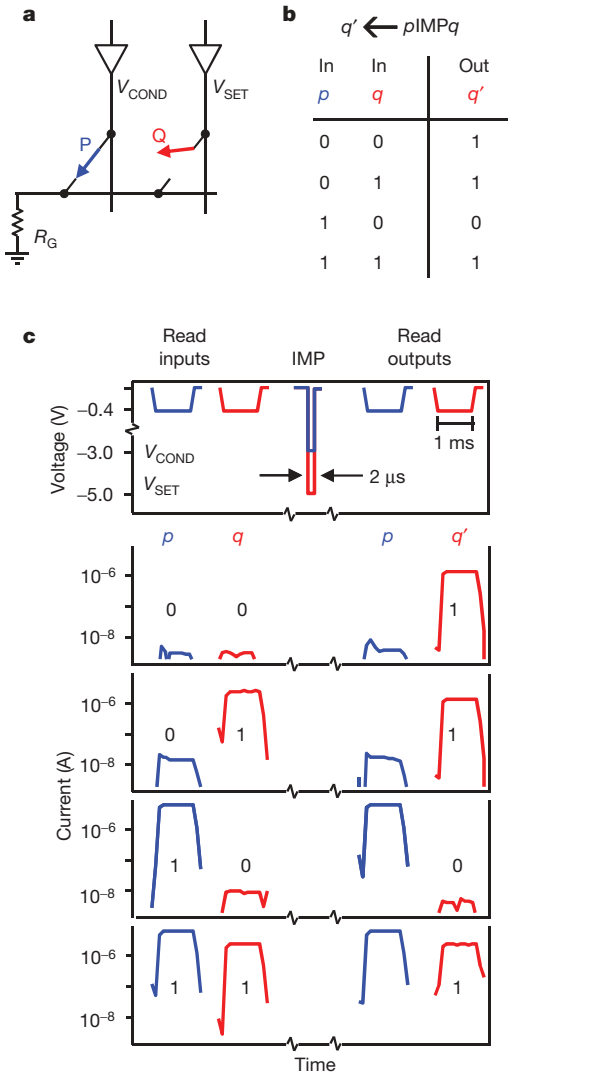

Figure 2 | Illustration of the IMP operation for the four input values of p and q. **a**, IMP is performed by two simultaneous voltage pulses, V_{COND} and V_{SET}, applied to switches P and Q, respectively, to execute conditional toggling on switch Q depending on the state of switch P. **b**, The truth table for the operation $q' \leftarrow p\mathrm{IMP}q$. **c**, The blue and red curves show the voltages applied and the absolute value of the currents read at junctions P and Q before and after the IMP voltage pulses. The measured low- and high-current values reproduce the IMP truth table.

V_{COND} pulse applied to P alone implements $p \leftarrow p$. Applied together, though, the two pulses interact through P, Q and the load resistor R_G to cause state changes that depend on the existing states of p and q: if P is in a high-resistance state ($p = 0$), it has little influence on the voltage divider formed by Q and R_G, and thus Q is set ($q \leftarrow 1$) while P is left unchanged ($p \leftarrow p$); but if P is in a low-resistance state ($p = 1$), the V_{COND} pulse on P 'shorts out' the voltage divider and both P and Q are left unchanged ($q \leftarrow q$, $p \leftarrow p$). Conditional toggling somewhat resembles the operation of resistor–transistor logic[23]. A resistor–transistor logic gate also uses a resistive voltage divider containing one or more 'variable resistors' (transistors) to compute a logic function: the transistors conditionally switch between high- and low-conductance states depending on the voltages applied to their bases, thus dynamically changing the relative resistance values and the output voltage of the voltage divider network.

The selection of R_G, which may be the resistance of an appropriate length of a nanowire, is important to the outcome of the operation. The resistance is chosen such that $R_{CLOSED} < R_G < R_{OPEN}$, where R_{CLOSED} and R_{OPEN} are the resistance states of the closed and open switches, respectively. When both P and Q are open, V_{COND} and

V_{SET}, respectively, drop mainly across each switch because $R_G < R_{OPEN}$; this leaves switch P open but closes switch Q. However, if switch P is closed, the voltage on the common wire is nearly V_{COND} since $R_{CLOSED} < R_G$, and thus the voltage drop across switch Q is approximately $V_{SET} - V_{COND}$, which leaves switch Q open. The robustness of this operation (see Supplementary Figs 1 and 2) relies on the margin between the common wire voltage modulation and the V_{SET} voltage dispersion. This margin is increased with a larger resistance switching ratio R_{OPEN}/R_{CLOSED}, but is degraded by the nonlinear current–voltage characteristic that is usually observed for memristive switches[13]. A further discussion of optimizing R_G to compensate for resistance nonlinearity in the switches is presented in Supplementary Fig. 3.

In an experiment demonstrating the IMP operation, shown in Fig. 2c, we first prepared P and Q by applying appropriate voltage pulses, V_{SET} or V_{CLEAR}, to initialize p and q to desired initial states; these states were verified by applying a small negative reading voltage of -0.3 V and measuring the resulting current to confirm that the desired values were stored in the switches. We then applied the simultaneous voltage pulses, V_{COND} and V_{SET}, to switches P and Q, respectively. By comparing the conditional toggling results of Fig. 2c to the truth table of Fig. 2b, we see that we successfully executed $q \leftarrow p\mathrm{IMP}q$.

Arbitrary logic computation requires a set of operations that are computationally complete. NAND is known to be universal, that is, any Boolean logic operation can be constructed from an appropriate network of NAND gates. Here we experimentally demonstrate that the latching IMP and FALSE operations are complete by synthesizing a NAND operation. This exercise also demonstrates how more complex compound logic operations would be executed with latching IMP logic. The operation $s \leftarrow p\mathrm{NAND}q$ was implemented in a circuit with three memristive switches, P, Q and S, as illustrated schematically in Fig. 3a. The computation was performed in three sequential steps:

$$s \leftarrow 0 \quad (1)$$

$$s' \leftarrow p\mathrm{IMP}s \quad (2)$$

$$s'' \leftarrow q\mathrm{IMP}s' \quad (3)$$

The inputs were the values p and q stored in switches P and Q, and the output was the value s'' accumulated in switch S. Experimental results for the three-step computation using three interconnected micrometre-scale memristive junctions are shown in Fig. 3 for the four possible p and q inputs 00, 01, 10 and 11. Initially, a V_{CLEAR} pulse was applied to switch S to execute $s \leftarrow 0$, the FALSE operation. All three junctions were then read at a voltage of -1.0 V to show the initial values of the three logic variables before the IMP operations. In the open state, each memristive device had a current of 10–100 μA (average 50 μA); the closed state allowed 600 μA–2.5 mA (average 1.5 mA). The second step, $s' \leftarrow p\mathrm{IMP}s$, was performed by applying a V_{COND} pulse to V_P simultaneously with a V_{SET} pulse to V_S. For the purposes of this demonstration, switch S was read at this point to show the intermediate result s'. The final operation, $s'' \leftarrow q\mathrm{IMP}s'$, was performed by applying a V_{COND} pulse to V_Q simultaneously with a V_{SET} pulse to V_S. All three junctions were read again, and their measured currents showed that each combination of initial inputs p, q correctly yielded the value of s'' that corresponded to the truth table for a NAND operation (Fig. 3b).

Other routes to achieving something similar to stateful logic have been to use spins for logic operations with magnetic tunnel junctions[4,5] or to combine a ferroelectric memory element in a configurable logic gate[6]. Previous nanoelectronic circuit proposals[23–28] have often described how maximum density crossbar arrays could be used for memory and conventional wired-AND or wired-OR logic circuits called programmable logic arrays. However, in practice these applications sacrifice the inherent density that is possible with crossbars because only a sparse set of junctions are usable, and they require a transistor to implement the NOT operation to be computationally complete. Instead of forcing these familiar Boolean logic schemes onto new nanoscale devices in doomed competition with ultrahigh-performance silicon integrated circuits, memristive IMP provides a

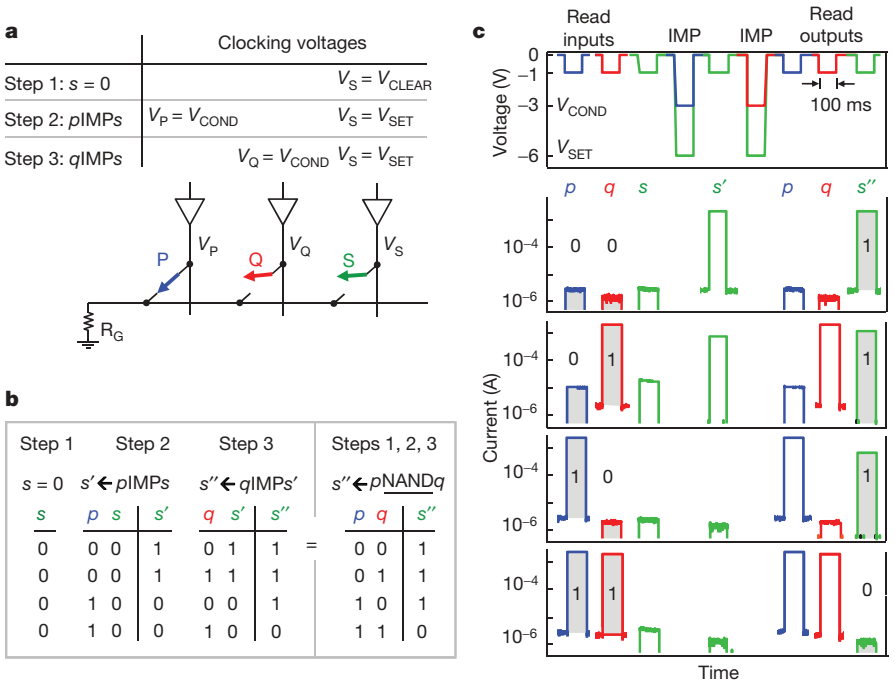

Figure 3 | The logic operation $s \leftarrow p\mathrm{NAND}q$ performed as a sequential operation with three memristive switches. **a**, The sequence of voltages applied to obtain the NAND operation with P, Q and S. **b**, The truth tables showing the equivalence of the sequence of operations to NAND. **c**, The experimental demonstration of the sequential NAND for all four input states of p and q. The blue, red and green curves display the applied voltage pulses and the absolute value of the measured current response for P, Q and S, respectively. The intermediate and final results are stored in S.

stateful logic that is an unconventional computation framework determined more by the nano-device properties than any pre-conceived logic architecture. Applications of this technology will most likely require substantial parallel operations in order to amortise any silicon-based driving circuitry (Supplementary Fig. 4). The devices themselves are capable of fast (nanoseconds) and low-energy (picojoules) switching (Supplementary Fig. 5) but further research will be required at the device, circuit and architecture levels to determine the practical utility of this approach. The major lesson from this research, however, is that when confronted with a new device, one needs to determine whether it has a natural basis for computation that is different from familiar paradigms.

METHODS SUMMARY

Sample fabrication was reported in detail in ref. 14 and is briefly summarized here. The memristor arrays comprise two layers of platinum wires that sandwich a 50-nm-thick active layer of TiO_2. The bottom metallic wire (1.5 nm of Ti followed by 8 nm of Pt) was formed by electron beam deposition onto a layer of nano-imprinted resist followed by lift-off[9,10]. Then, a uniform layer of titanium dioxide was deposited over the entire substrate, held at 250 °C, by sputtering from a rutile target in 3 mtorr Ar. Finally, the top 11-nm-thick Pt wires were fabricated using the same process as the bottom wire. The as-fabricated switches were highly resistive; they were subjected to an electrical forming step to enable them to switch[29]. For the NAND demonstration, we used micrometre-scale junctions (wire width ~10 μm) to reduce the series resistance of the wires to a level that would be more typical in an integrated circuit with memristive switches and active driving circuitry in close proximity. The smaller series resistance of the wire increased the effective switching ratio and therefore simplified the requirements (see Supplementary Fig. 3) for the applied voltages and R_G.

The quasi-direct-current electrical characteristics were measured with a Semiconductor Parameter Analyser (Hewlett-Packard HP4155). The pulsed measurements were made with a voltage source (National Instruments NI6733) and a current amplifier (Stanford Research Systems SR570). The junctions were connected through an external switching matrix (Keithley 707A) to the instruments, ground or a high impedance to simulate the tri-state voltage driver. When a junction resistance was measured, the other junctions were connected to the high impedance using the switching matrix. The blanks between the voltage pulses in Figs 2 and 3 represent the external matrix reconfiguration delay (3 s).

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